Challenges in Energy-Efficient Memory Architecture

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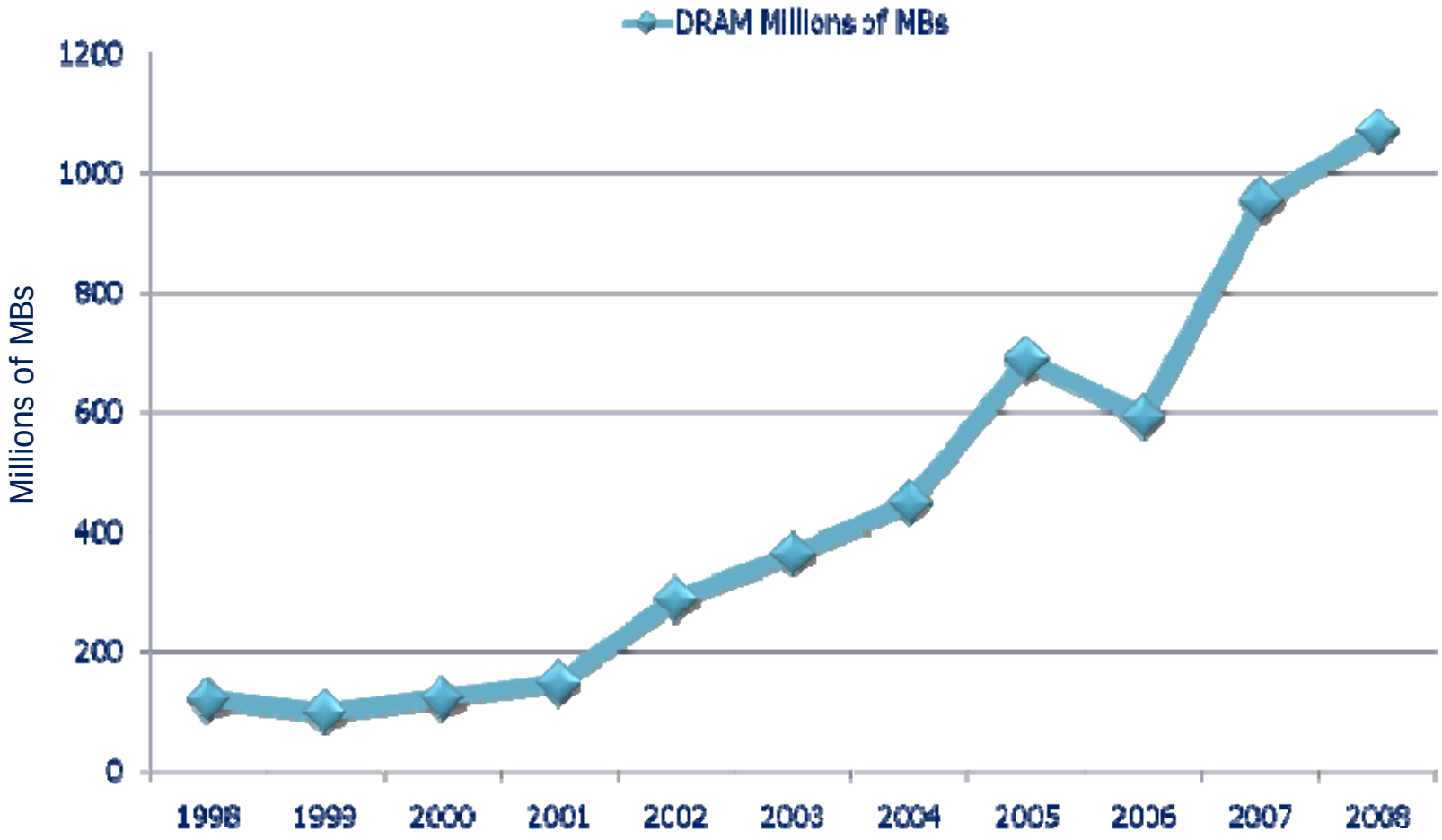
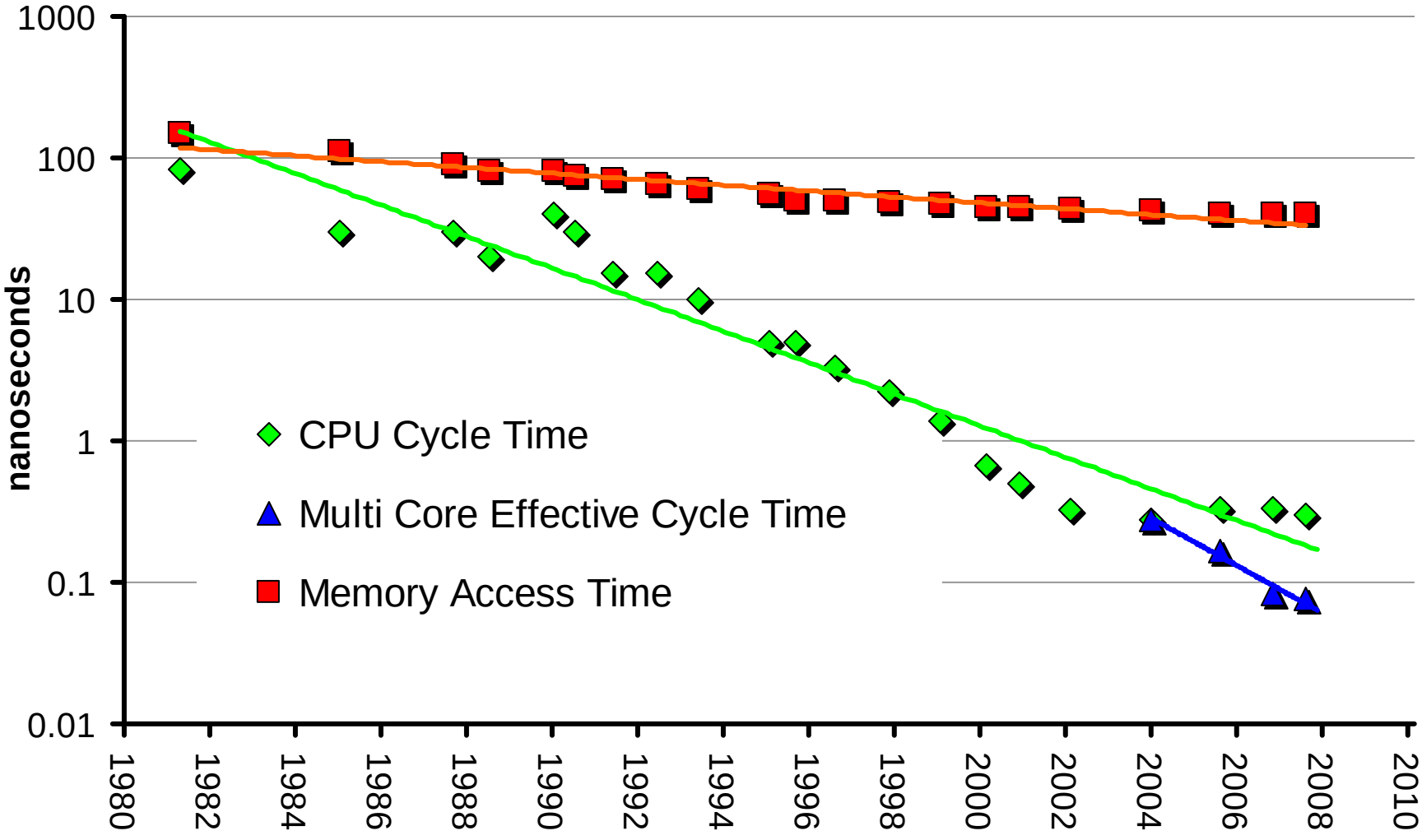
Bigger Computers
+ Bigger Programs
+ Bigger Datasets
==========
More Memory

High End Server Systems

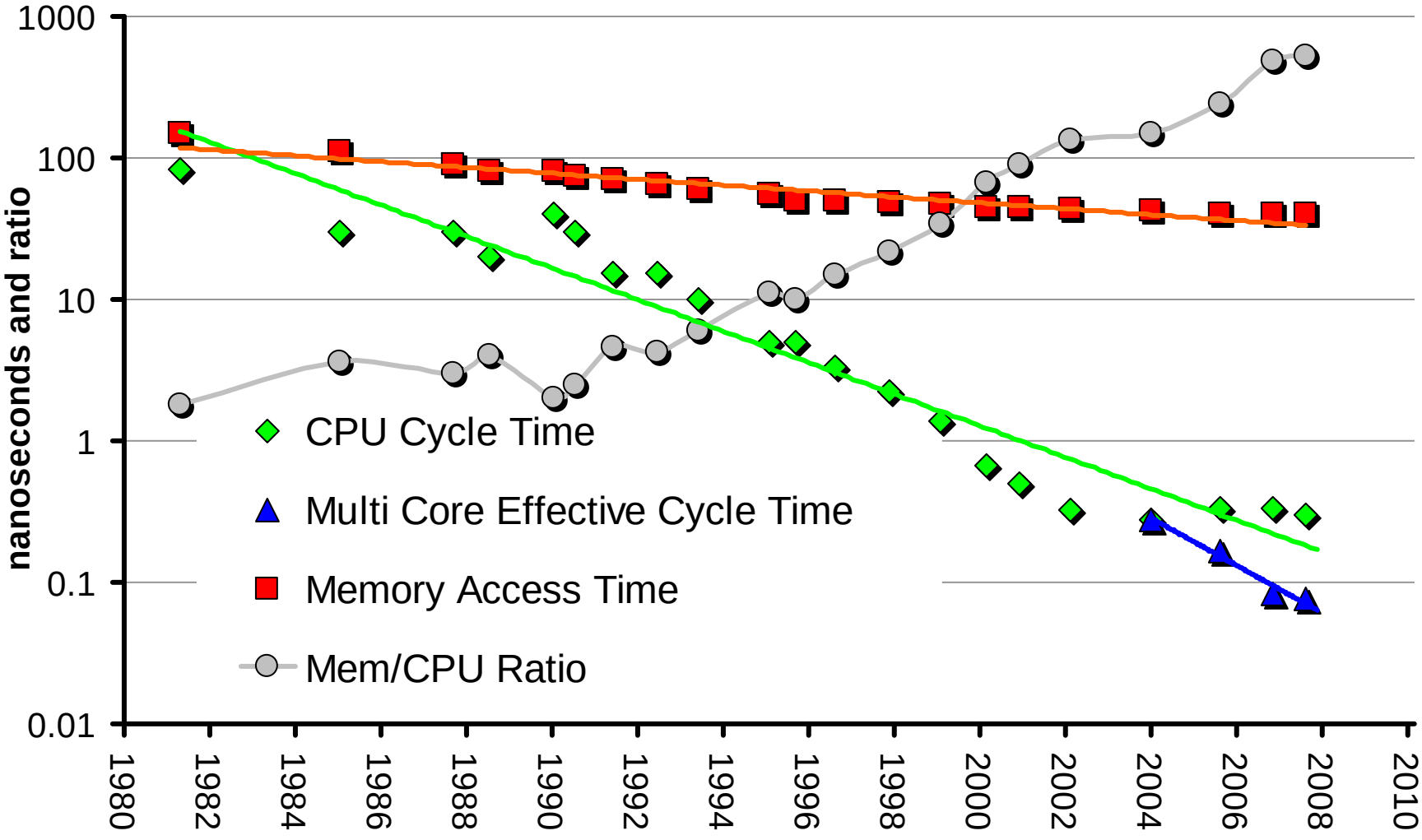


Note: IDC defines High End Servers as those severs that cost greater than $500K

Memory as the Bottleneck



Memory as the Bottleneck



More Memory = More Power

Servers: Recognizing Memory Power Consumption

According to the Environmental Protection Agency (EPA), data centers consumed about 60 billion kilowatt-hours (kWh) in 2006, roughly 1.5 percent of total U.S. electricity consumption.

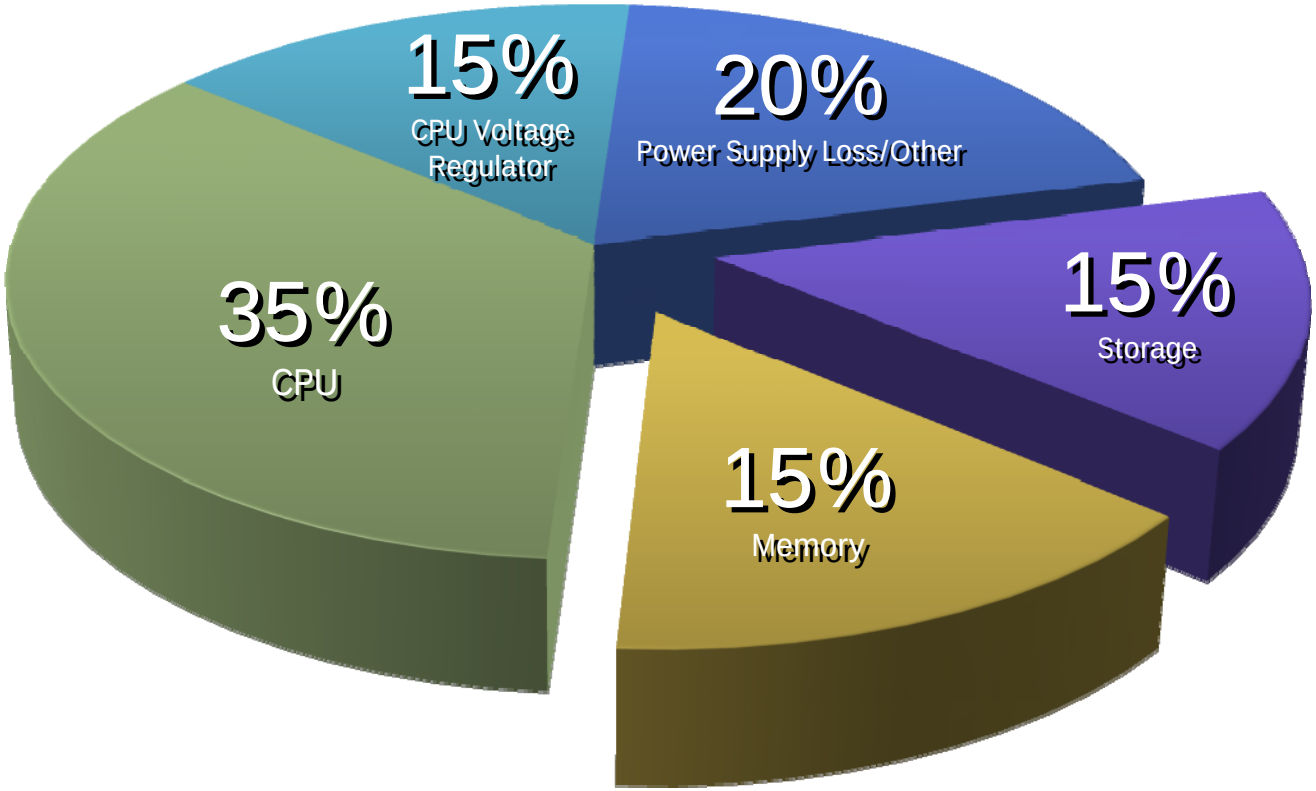
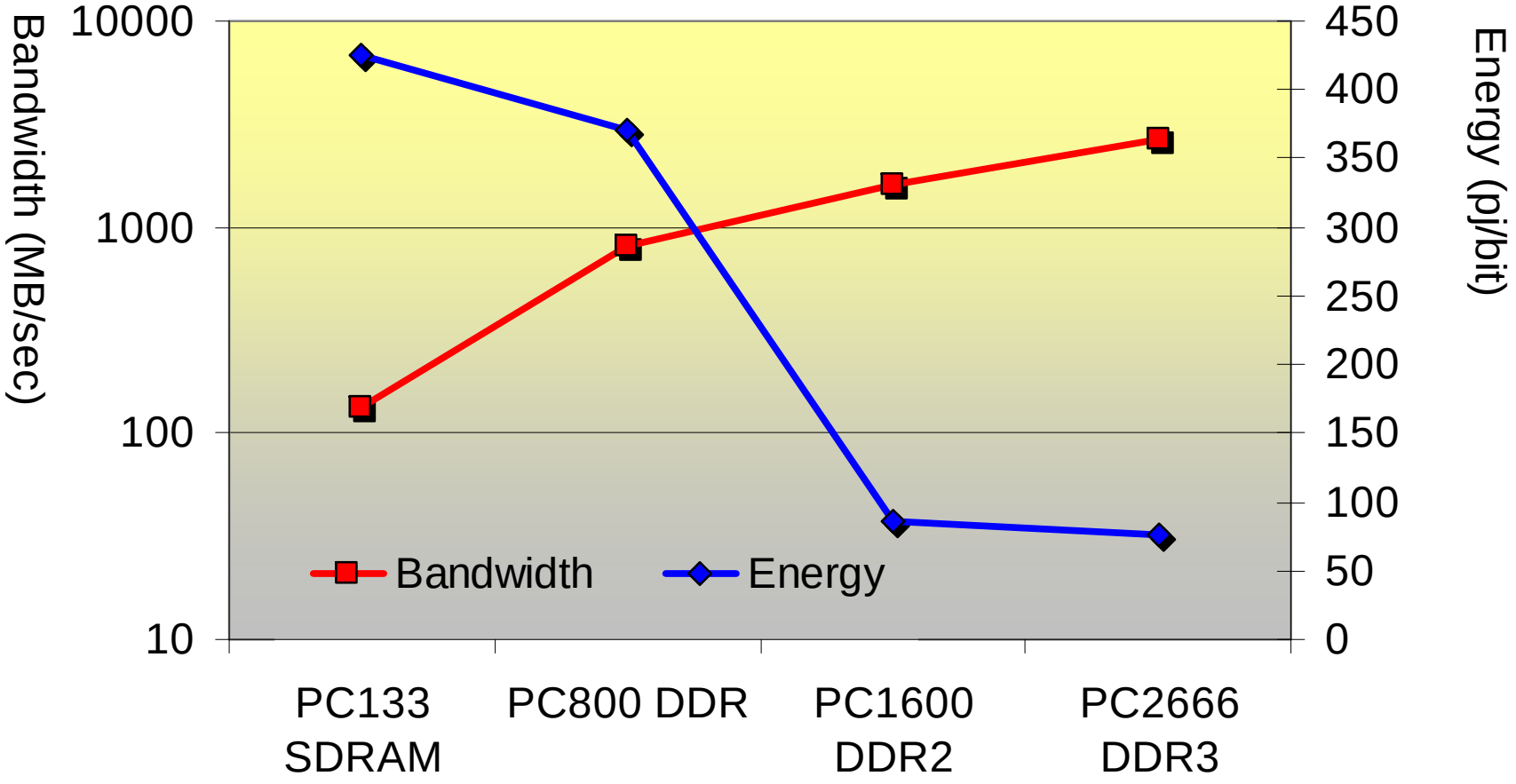
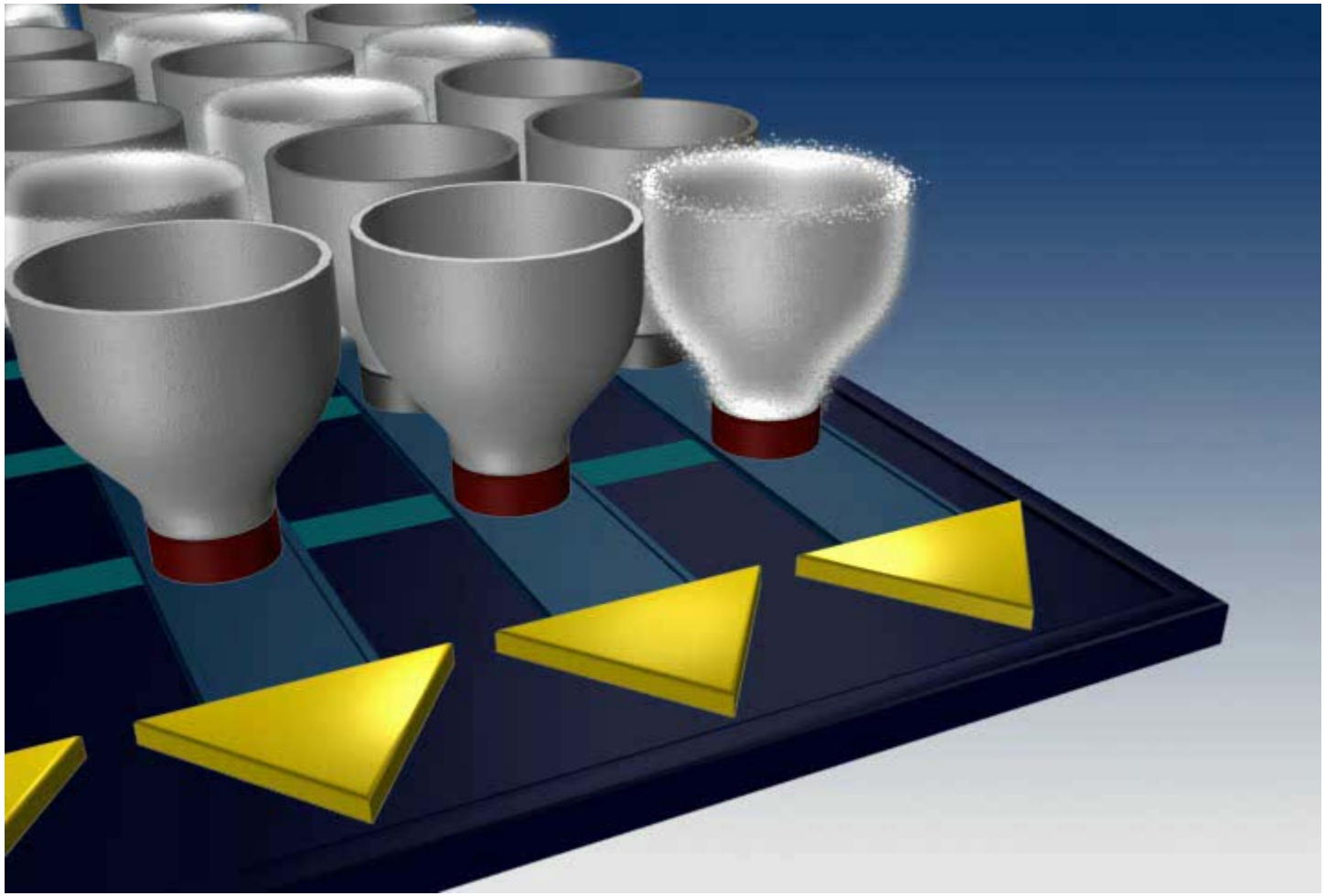


Chart does not include HVAC requirements.

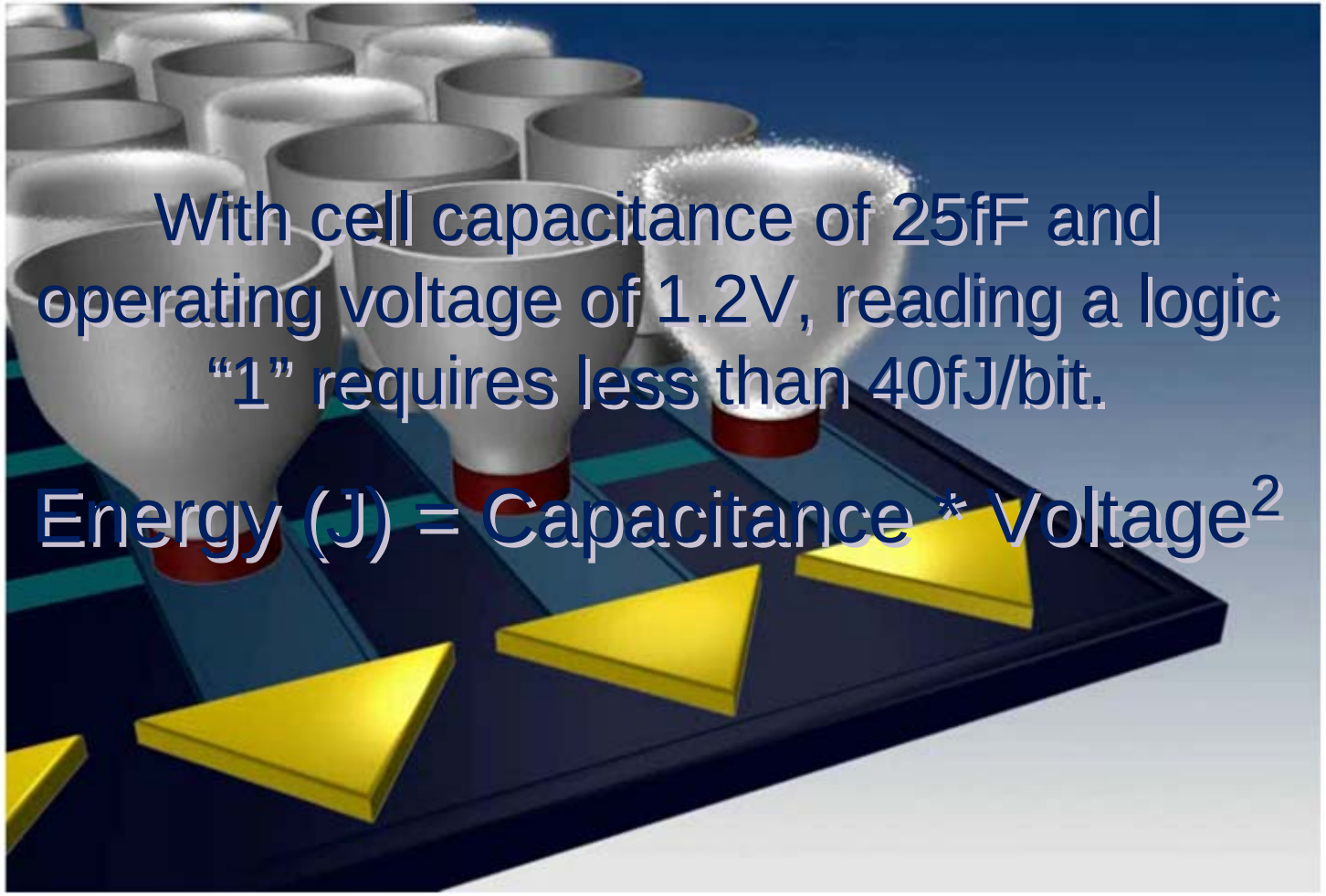
Memory Power Evolution



Understanding DRAM Power



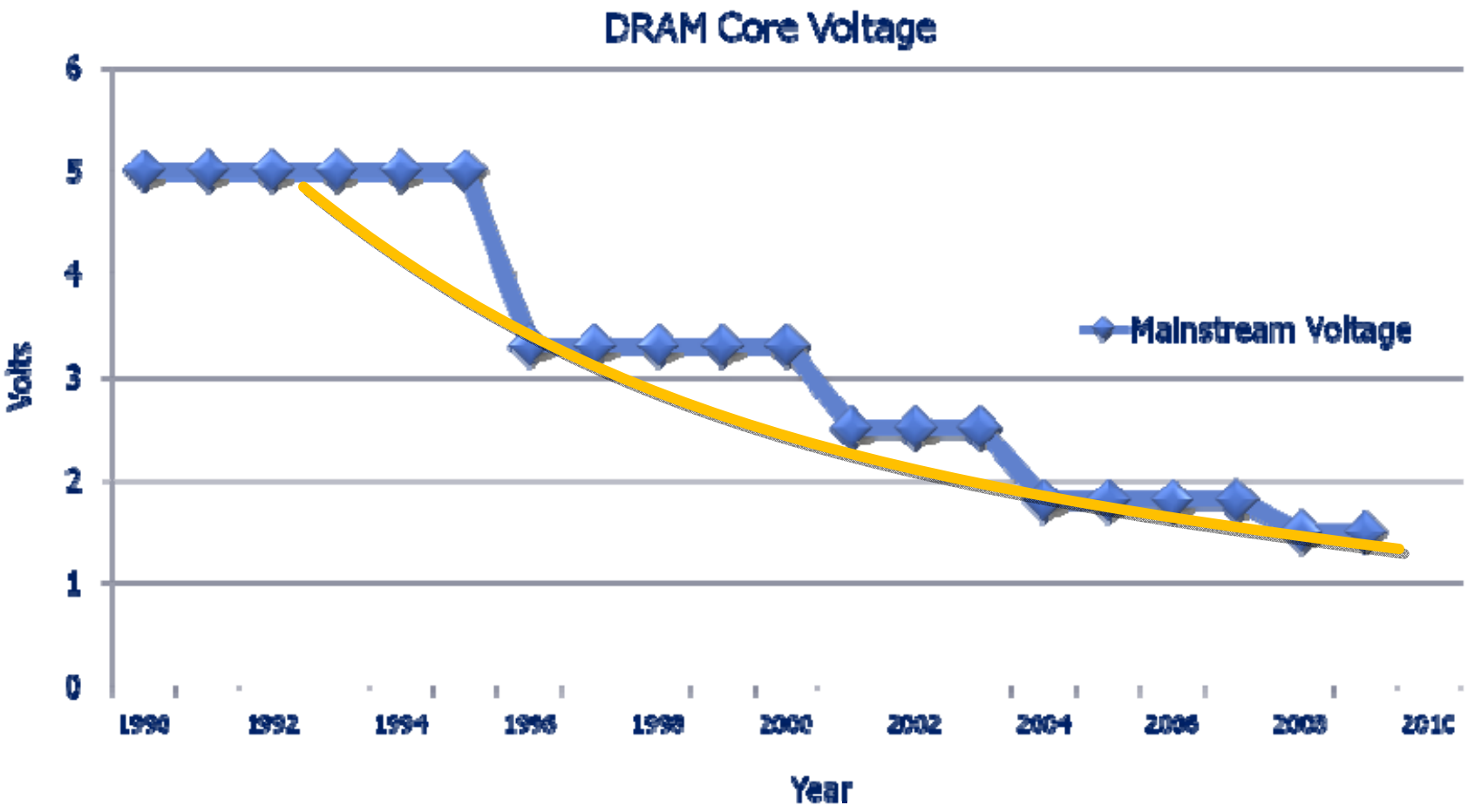
Understanding DRAM Power



With cell capacitance of 25fF and operating voltage of 1.2V, reading a logic "1" requires less than 40fJ/bit.

Energy (J) = Capacitance * Voltage^2

Voltage Scaling Slowing



Exascale: The Power of Memory

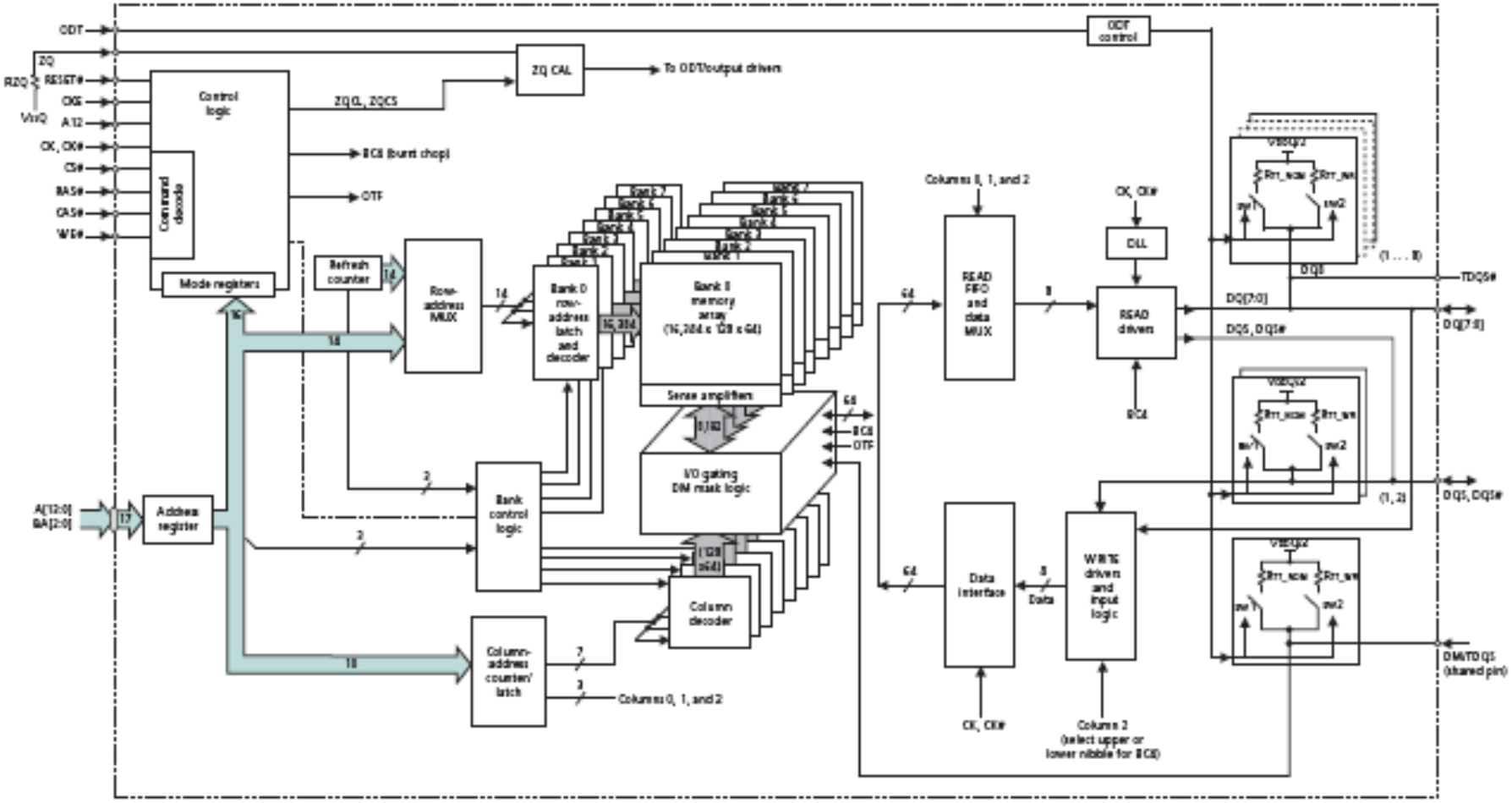
Assumptions

Cell Voltage	1.2	V
Cell Capacitance	25	fF
Bitline Capacitance	75	fF
Memory System Bandwidth	1	EB/sec

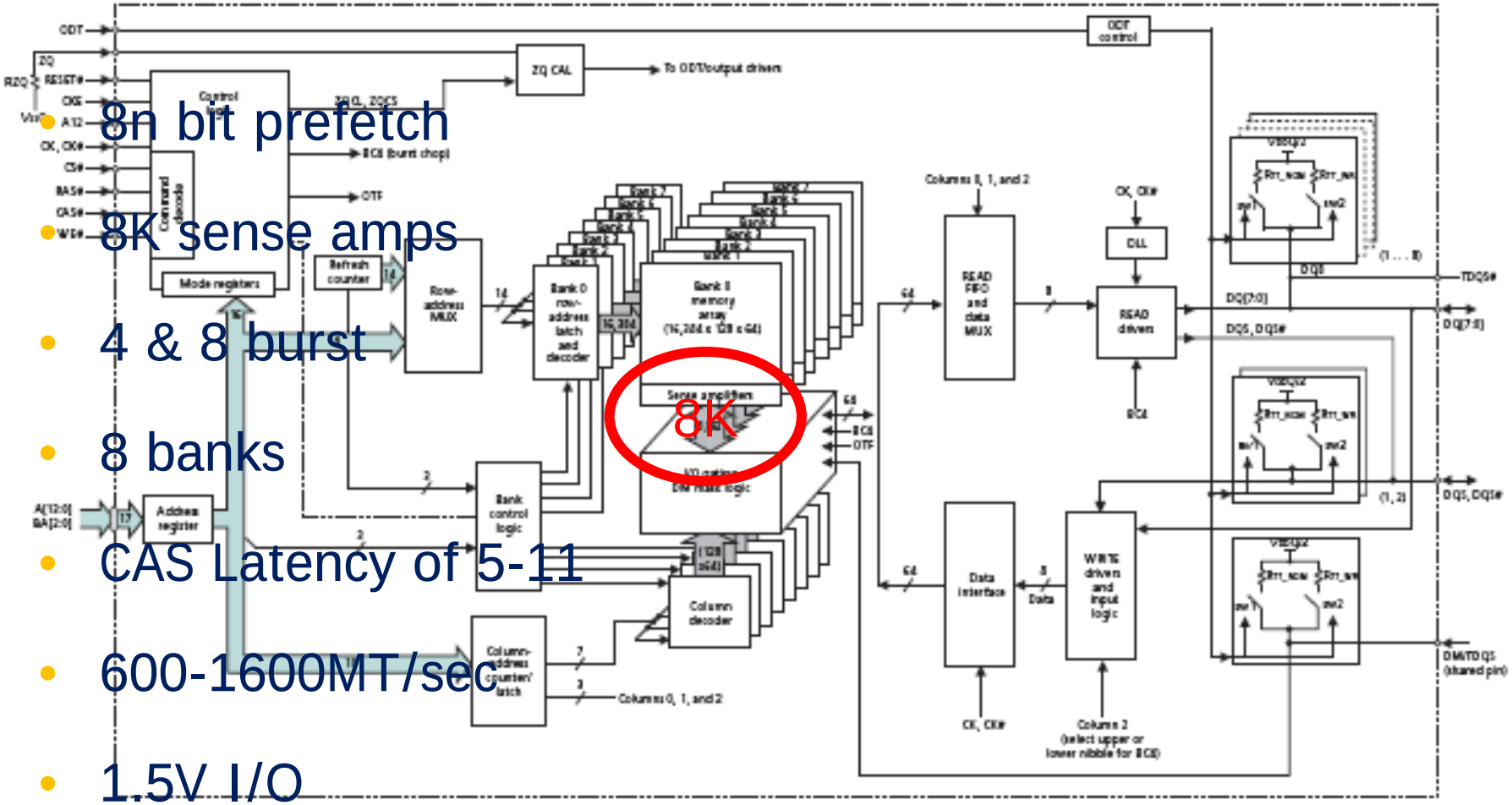
Simplified Results:

Energy/bit	36	fJ
Total Memory Cell Power	288	KW
With Bitline	1150	KW
With 512X Over-Fetch	590	MW

1Gbit DDR3 Architecture



1Gbit DDR3 Architecture

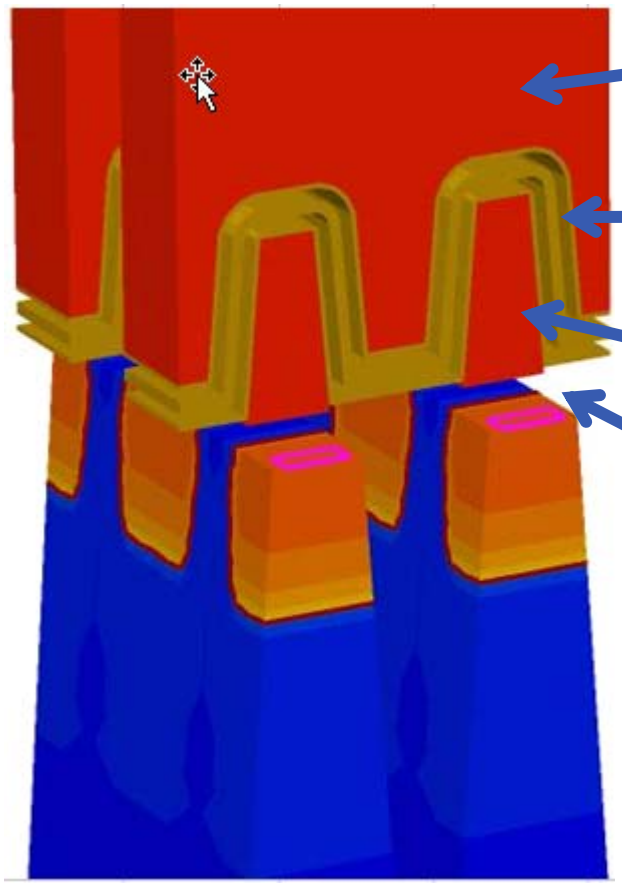


- 8n bit prefetch
- 8K sense amps
- 4 & 8 burst
- 8 banks
- CAS Latency of 5-11
- 600-1600MT/sec
- 1.5V I/O

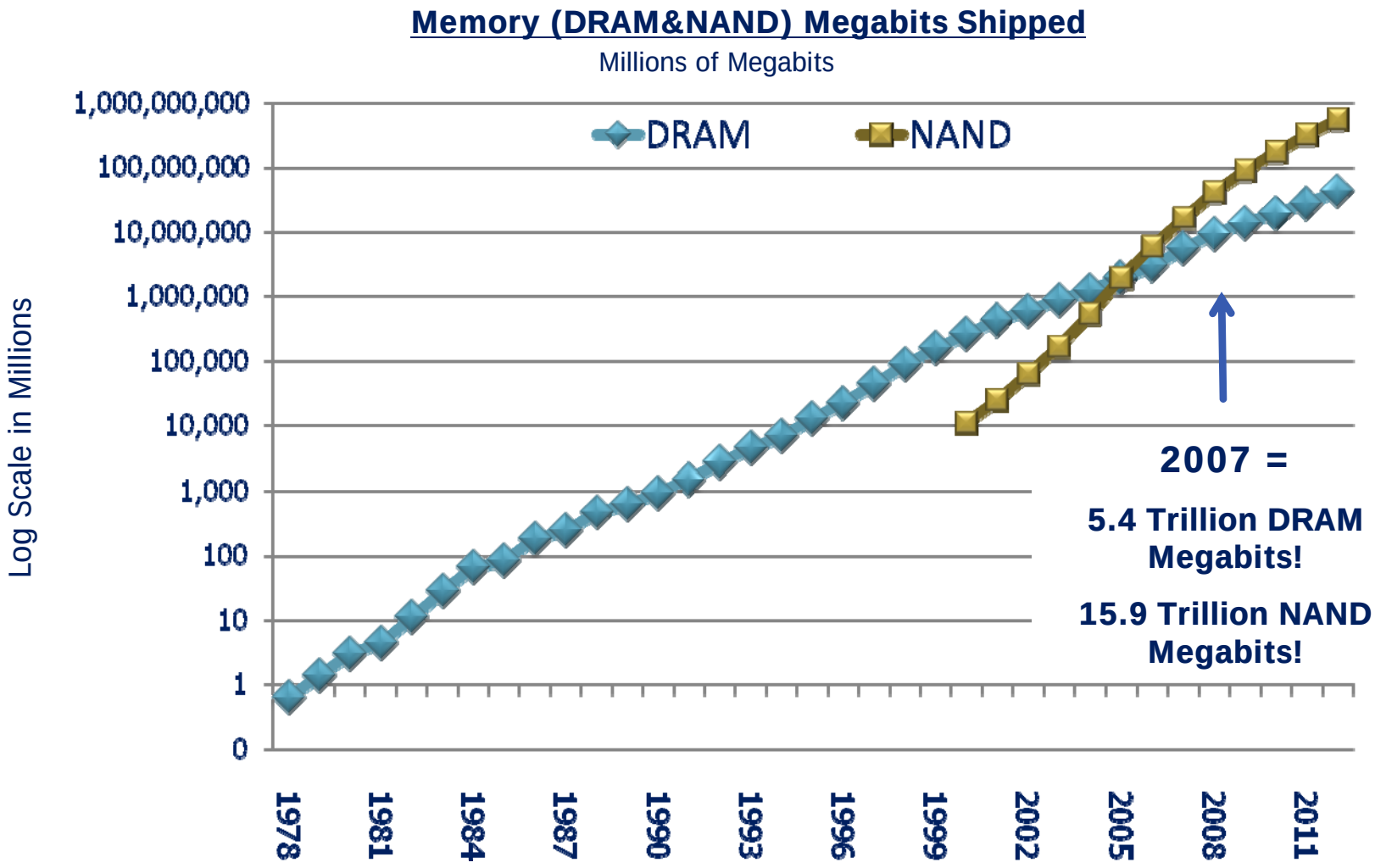
Viable Alternatives?

Cell Size (u^2)	Tech Node (nm)	Cell size (F^2)	Endurance	SEU Susceptability
IBM/Infineon MRAM				
0.74	130	44	Excellent	Excellent
Freescale 6T-SRAM				
0.69	65	163	Excellent	Poor
Intel 45nm 6T-SRAM				
0.27	45	135	Excellent	Poor
Samsung 512Mbit PRAM Device				
0.050	95	5.5	1E7??	Excellent
Micron 50-series DRAM				
0.024	63	6	Excellent	Excellent
Micron 60-series NAND				
0.0046	34	4	1E5	Excellent
0.0023	34	2	1E4	Excellent

NAND - A Floating Gate Cell



Despite a Later Start, NAND Overtook DRAM in Bit Shipments in 2006



Source: Gartner

NAND in Computing

NAND

CPU

Relative Latency		Relative Cost/bit
1	L1 Cache	1,800
2.5	L2 Cache	1,400
600	DRAM	10
25,000	SSD	3

NAND Flash Closes the Latency Gap

Cost/bit Data as of November 2007

The Power of Solid-State Storage

Becoming a Reality?

Evolutionary (JEDEC) memory path severely limits improvements in power and performance.

- Power is wasted in over-fetch
- Voltage scaling is slowing
- Architecture not multi-core “friendly”

Proven memory cells can scale

- New DRAM architectures can deliver more performance for less power
- NAND has a place in the architecture

Industry-wide economic challenges are an obstacle

- Sell it at a loss... Hasn’t changed.

Questions?

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